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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte KOKHOE CHIA, MYINT NGWE, JINQUAN SHEN, and
SWEEKIEONG CHOO

Appeal 2008-0211
Application 10/664,611
Technology Center 2100

Decided: May 27, 2008

Before JEAN R. HOMERE, JAY P. LUCAS,
and THU A. DANG, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal under 35 U.S.C. § 134 from the Examiner's rejection of claims 15 through 17. Claims 1, 2, 4 through 10, and 12 through 14 have been allowed. Claims 3 and 11 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We affirm.

The Invention

Appellants invented a method and system for reclaiming unused buffer space in a random access memory (RAM). (Spec. 1.) As depicted in Figure 2, the RAM (251) includes a first buffer portion (253) for storing therein a defect table. The RAM (251) also includes a second buffer portion (254) allocated for caching data. Upon determining the amount of memory space that the defect table actually occupies in the first buffer portion (253), a microcontroller (240) reallocates to the second buffer portion (254) any unused space remained in the first buffer portion (253). (Spec. 7.)

Independent claim 15 further illustrates the invention. It reads as follows:

> 15. A method of managing a buffer random access memory, the buffer random access memory having a first portion allocated for a defect table and a second portion allocated for data caching, the method comprising:
>
> determining actual memory space of the first portion of the buffer random access memory which is actually occupied by the defect table in order to identify unused memory space of the first portion; and
>
> reallocating the unused memory space of the first portion of the buffer random access memory for use in data caching.

. In rejecting the claims on appeal, the Examiner relies upon the following prior art:

Tsuchimoto	US 6,336,202 B1	Jan. 01, 2002

The Examiner rejects the claims on appeal as follows:
Claims 15 through 17 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tsuchimoto.

FINDINGS OF FACTS

The following findings of facts (FF) are supported by a preponderance of the evidence.

Tsuchimoto

1. Tsuchimoto discloses a method and system for reducing the size of a memory region containing defects encountered in a RAM (14). (Abstract, col. 5, ll 15-18.)

2. As depicted in Figure 6, Tsuchimoto discloses a storage medium within the RAM (14) having a map for recording the logical block address (LBA) of each defect area therein as well as the length thereof. (Col. 2, ll. 18-23, col. 3, ll. 38-50.)

3. Tsuchimoto discloses that storage blocks other than the defective sectors identified on the map are used to for writing or caching data. (Col. 2, ll. 23-25.)

PRINCIPLES OF LAW

ANTICIPATION

In rejecting claims under 35 U.S.C. § 102, "a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis*

Pharmaceutical Corp., 432 F.3d 1368, 1375-76 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565 (Fed. Cir. 1992). "Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (Internal citations omitted).

ANALYSIS

Independent claim 15 recites in relevant part determining the actual memory space that a defect table occupies in a first buffer portion of a RAM and reallocating any unused space in the first buffer portion for caching data. (App. Br. 10, Claims Appendix.) Appellants argue that Tsuchimoto does not teach the recited limitations. (App. Br. 6-8.)

The Examiner, in response, finds that Tsuchimoto's disclosure of identifying on a defect map the addresses and length of memory defects in a RAM to enable writing or caching data in the remaining memory areas that are not on the map inherently teaches the claimed invention. (Ans. 3-5, and 7-9.)

Thus, the pivotal issue before us is whether one of ordinary skill in the art would find that Tsuchimoto's disclosure of identifying on a defect map the address and length of defect sectors in a RAM teaches determining the actual memory space that a defect table occupies in a RAM to reallocate

unused areas in a first buffer portion for caching data, as claimed. We answer this inquiry in the affirmative.

As detailed in the Findings of Facts section above, Tsuchimoto discloses identifying on a defect map the location and length of defect areas in a RAM. (FF. 2.) Tsuchimoto further discloses writing or caching data to areas other than those identified on the defect map. (FF. 3.) One of ordinary skill in the art would readily recognize that Tsuchimoto's map, by identifying the addresses and lengths of defective memory areas on the RAM, depicts thereon the actual memory space that such defective sectors actually occupy in the aggregate. Further, the ordinarily skilled artisan would aptly recognize that Tsuchimoto, by allowing the user to write to memory areas other than those previously identified on the defect map, implicitly teaches that any LBAs not corresponding to those on the map (i.e. the first buffer portion) can be allocated for caching data. Accordingly, the ordinarily skilled artisan would duly appreciate that, by designating any buffer area on the RAM that is not featured on the defect map as a cacheable area, Tsuchimoto necessarily teaches that any such unused areas in any portion of the RAM are to be reclaimed, and reallocated for caching purposes.

"In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). "[A]fter the PTO establishes a prima facie case of anticipation based on inherency, the burden shifts to

appellant to 'prove that the subject matter shown to be in the prior art does not possess the characteristic relied on.'" *In re King*, 801 at 1327(Fed. Cir. 1986) (quoting *In re Swinehart*, 439 F.2d 210, 212-13, (CCPA 1971)). *See also* MPEP §§ 2112 (IV.), (V.).

This reasoning is applicable here. We agree that the Examiner has properly shifted the burden to Appellants by providing a rationale in the Answer that reasonably supports the Examiner's finding of inherent anticipation with respect to the Tsuchimoto reference. In response, Appellants merely allege that Tsuchimoto's disclosure does not necessarily teach determining the actual memory space that a defect table occupies in a first buffer portion of a RAM to reallocate any unused space in the first buffer portion for caching data. (App. Br. 6-8.) Appellants' mere allegations are insufficient to prove that the subject matter shown to be in the prior art does not possess the characteristic relied on by the Examiner. It follows that Appellants have not shown that the Examiner erred in finding that Tsuchimoto anticipates independent claim 15.

Appellants do not provide separate arguments with respect to the rejection of claims 16 and 17. Therefore, we select claim 15 as being representative of the cited claims. Consequently, claims 16 and 17 fall together with representative claim 15. 37 C.F.R. § 41.37(c)(1)(vii).

SUMMARY and DECISON

Appellants have not shown that the Examiner erred in concluding that Tsuchimoto anticipates claims 15 through 17 under 35 U.S.C. § 102(b). Claims 15 through 17 are unpatentable. Therefore we affirm this rejection.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

pgc

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